

Fault tolerant quantum computing R&D | PATHFINDER

NQCP LADDER

- A6. Usecases
- A5. Experiments / simulations
- A4. Models
- A3. Algorithms
- A2. Algorithm to circuit
- A1. Resource estimation

HW resource estimation for a given Quantum Algorithm

QA width (#N logical qubits) and depth (#N seq. operations)

A&A

9. Applying FTQC

8. Interconnects

7. QPU (single unit)

6. Universal gate set (logic)

HW

5. Logic gate operations

4. Error correction

3. Parity check (Error detection)

2. Qubits (physical)

1. Materials / subsystems

PULL / INFORM

PUSH / ENABLE

SUB-LEVEL TRL / METRICS OF INTEREST

